



SHEET 1 OF 1

INFORMATION DISCLOSURE
CITATION IN AN
APPLICATION

(PTO-1449)

ATTY. DOCKET NO.
60188-044SERIAL NO.
09/810,518APPLICANT
Hirokazu YONEZAWA, et al.FILING DATE
March 19, 2001GROUP
2423 2128

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes - Number - Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation	
						Yes	No
RF		JP 11-219380 A (w/ English Abstract)	08/10/1999	MATSUSHITA ELECTRIC IND. CO., LTD.	—		

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
RF		Y. KAWAKAMI et al., "Gate-Level Aged Timing Simulation Methodology for Hot-Carrier Reliability Assurance", Proc. ASP-DAC 2000, IEEE, January 28, 2000, pages 289-294.

EXAMINER

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